

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30

TITLE OF THE INVENTION

Liquid Crystal Display Apparatus and Method of Driving LCD Panel

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a liquid crystal display apparatus and a method of driving a liquid crystal display panel.

Description of the Related Art

A liquid crystal display panel comprises a matrix array of pixels each being formed by a switching transistor and a liquid crystal cell. All switching transistors are connected to intersections of column lines and row lines which are successively selected. When one of the row lines is selected, the column lines are respectively driven by write-in voltages. With the advancing technology in the field of flat panel displays, the recent tendency is toward developing large sized, high definition display panels. As the screen size increases, the write-in voltages must travel through the increased length of the column lines. Since the write-in voltages are supplied to the liquid crystal cells of the selected row line for a fixed write-in period, they suffer from undesirable attenuation and distortion, causing different shades of gray to occur between the top and bottom of the screen as illustrated in Fig. 1.

To overcome this problem, Japanese Patent Publication 2002-182616 discloses a technique whereby variable supplemental voltages are generated and combined with write-in voltages. The combined voltages vary increasingly with the distance between the selected row line to the end points where the combined voltages are supplied.

However, because of the analog circuitry, difficulty arises to provide precision circuit adjustment. Therefore, a need exists to provide a solution whereby circuit adjustment can be easily and precisely performed on liquid crystal display apparatus.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a liquid

1 crystal display apparatus and a method of driving a liquid crystal display
2 panel by controlling the write-in period according to different distances
3 traveled along the column lines by the write-in voltages. Since the pulse
4 duration can be easily controlled by digital circuitry, the present invention
5 solves the problem of different shades of gray across the screen of a liquid
6 crystal display.

7 According to a first aspect of the present invention, there is provided a
8 liquid crystal display apparatus comprising a liquid crystal display panel a
9 liquid crystal display panel comprising a matrix array of transistors and a
10 matrix array of liquid crystal cells respectively connected to the transistors,
11 the transistors being respectively connected to intersections of a plurality of
12 column lines and a plurality of row lines for activating the liquid crystal cells,
13 and a driving circuit for successively generating a plurality of write-in
14 voltages of a line signal of a video frame at end points of the column lines,
15 successively selecting each of the row lines and supplying the write-in
16 voltages from the end points of the column lines to the liquid crystal cells of
17 the selected row line for a variable write-in period corresponding to a
18 geometric distance from the selected row line to the end points. The write-in
19 period may be increasingly variable from a nominal value or increasingly
20 variable from a less-than-nominal value to the nominal value or a
21 combination of both.

22 According to a second aspect, the present invention provides a method
23 of driving a liquid crystal display, wherein the liquid crystal display panel
24 comprises a matrix array of transistors and a matrix array of liquid crystal
25 cells respectively connected to the transistors, the transistors being
26 respectively connected to intersections of a plurality of column lines and a
27 plurality of row lines for activating the liquid crystal cells. The method
28 comprises the steps of (a) generating a plurality of write-in voltages of a line
29 signal of a video frame so that the write-in voltages appear at end points of
30 the column lines, (b) successively selecting one of the row lines, and (c)

1 successively supplying the write-in voltages from the end points of the
2 column lines to the liquid crystal cells of the selected row line for a write-in
3 period corresponding to the geometric distance from the selected row line to
4 the end points.

5 BRIEF DESCRIPTION OF THE DRAWINGS

6 The present invention will be described in detail further with reference
7 to the following drawings, in which:

8 Fig. 1 is a graphic representation of a prior art liquid crystal display
9 panel in which luminance values are plotted as a function of time to illustrate
10 a luminance error between the first and last lines;

11 Fig. 2 is a block diagram of an LCD drive circuit according to a first
12 embodiment of the present invention;

13 Fig. 3 is a block diagram of the timing controller of Fig. 2;

14 Fig. 4 is a timing diagram of the operation of Fig. 3;

15 Fig. 5 is a graphic representation of the luminance-versus-time
16 characteristics of the first embodiment of the present invention;

17 Fig. 6 is a block diagram of an LCD drive circuit according to a second
18 embodiment of the present invention;

19 Fig. 7 is a block diagram of the timing controller of Fig. 6;

20 Fig. 8 is a timing diagram of the operation of Fig. 6;

21 Fig. 9 is a graphic representation of the luminance-versus-time
22 characteristics of the second embodiment of the present invention;

23 Fig. 10 is a block diagram of an LCD drive circuit according to a third
24 embodiment of the present invention;

25 Fig. 11 is a block diagram of the timing controller of Fig. 10;

26 Fig. 12 is a timing diagram of the operation of Fig. 10; and

27 Fig. 13 is a graphic representation of the luminance-versus-time
28 characteristics of the third embodiment of the present invention.

29 DETAILED DESCRIPTION

30 Referring now to Fig. 2, there is shown an LCD drive circuit according

1 to a first embodiment of the present invention. The drive circuit comprises a
2 column driver 2 and a row driver 3 for respectively driving a liquid crystal
3 display panel 1 in response to timing pulses supplied from a timing controller
4 4. In the first embodiment, the vertical blanking interval of each frame is
5 utilized to stretch gate control pulse longer than the usual gate-on time. For
6 this purpose, a buffer memory 5 is provided for temporarily storing video
7 input data from an external source, not shown. The stored video data is
8 supplied line-by-line to the column driver 2. Input timing signal (sync and
9 clock) is also supplied from the external source to the timing controller 4.

10 The LCD panel 1 is comprised of a plurality of column (drain) lines 10
11 connected to the column driver 2 for receiving video signals, a plurality of
12 horizontal row (gate) lines 11-1 ~ 11-N connected to the row driver 3 for
13 receiving a gate control pulse. A matrix array of picture elements (pixels) are
14 located at intersections of the column lines 10 and the row lines 11. Each
15 pixel comprises a thin-film transistor 12 and a liquid crystal cell 13. In each
16 pixel, the transistor 12 connects its drain to the associated column line 10 and
17 its gate to the associated row line 11, and the liquid crystal cell 13 is
18 connected between the source of the transistor 12 and a common electrode 14.

19 As will be described below, the gate control pulse is shifted from one
20 row line to the next in response to a gate drive clock pulse (VCK) from the
21 timing controller 4. The duration of each gate control pulse begins at the
22 leading edge of a VCK pulse and ends at the leading edge of the next VCK
23 pulse. In the presence of a gate control pulse, a line signal of a video frame
24 supplied to the column driver 2 is latched in response to a data latch pulse
25 (DLP). A "write-in period" of a selected row line is defined between the
26 trailing edge of a DLP pulse and the leading edge of a VCK pulse for writing
27 the latched line signal into the liquid crystal cells 13 of a selected row line 11.
28 By increasing varying the interval between successive VCK pulses according
29 to the geometric distance from a selected row line to the column driver 2
30 along the column lines 10, the write-in period is increasingly varied as the

1 point of selection proceeds from the row line 11-1 to the row line 11-N.

2 All liquid crystal cells 13 are air-tightly sealed in a transparent flat
3 panel, not shown, and the column lines 10, the row lines 11 and the
4 transistors 12 are arranged on one side of the flat panel and the common
5 electrodes 14 and a color filter are arranged on the other side. Each liquid
6 crystal cell 13 corresponds in position to each dot of the screen and is capable
7 of charging a "write-in" voltage supplied from the column driver 2 when the
8 associated switching transistor 12 is turned on in response to a gate control
9 pulse from the row driver 3. When the transistor 12 is turned off at the
10 trailing edge of the gate control pulse, the associated liquid crystal cell 13
11 holds the write-in voltage until the end of a frame period.

12 All the common electrodes 14 are usually biased at a constant voltage
13 of 7 volts. Using this bias voltage as a reference, the polarity of the write-in
14 voltage is determined. Usually, a positive write-in voltage varies in the range
15 between 8 and 13 volts and a negative write-in voltage varies in the range
16 between 1 and 6 volts. Thus, the write-in voltage varies in a range from 1 to 6
17 volts on either side of the 7-volt reference voltage.

18 In the first embodiment, the column driver 2, also known as a source
19 driver, includes a shift register 20, a latch circuit 21 and a conversion circuit
20 22. Shift register 20 responds to a start pulse (SP) from the timing controller 4
21 for receiving video data which is serially clocked pixel-by-pixel in response to
22 a dot clock pulse (DCK). When all pixel data of a line are clocked into the
23 shift register 20, they are supplied in parallel to the latch circuit 21 in
24 response to the leading edge of a data latch pulse (DLP) from the timing
25 controller 4. Conversion circuit 22 performs the conversion of individual
26 pixel data into write-in voltages and drives the column lines 10 with the
27 write-in voltages via appropriate impedance matching circuits.

28 Row driver 3, which is also known as a gate driver which responds to
29 the start pulse (SP) and a gate-drive clock pulse (VCK) from the timing
30 controller 4 for sequentially selecting the row lines 11-1 ~ 11-N so that each

1 row line is selected between the leading edge of the corresponding VCK
2 pulse and the leading edge of the next VCK pulse. For each row line 11-i (i=1,
3 2, ...N), each of the SP, VCK and DLP pulses is generated at intervals
4 increasingly variable as a function of the geometric distance along the column
5 lines 10 from the selected row line 11-i to the column driver 2.

6 As shown in Fig. 3, the timing controller 4 of the first embodiment
7 comprises a sync detector 40 for discriminating the input clock and sync
8 timing signals to detect the frame sync and line sync timing of the input
9 video frame and produces a dot clock pulse DCK. A line counter 41, which is
10 reset when a frame sync is detected, increments a count number each time a
11 line sync is detected and provides a binary line-count number to a memory
12 42. Write-in additive timing values $0, \alpha_1$ through α_{N-1} are stored in the
13 memory 42, respectively corresponding to row lines 11-1, 11-2 through 11-N.
14 Each of the additive timing values α_1 through α_{N-1} is determined as a
15 function of the geometric distance from a corresponding one of the row lines
16 11-2 ~ 11-N to the column driver 2 along the column lines 10. Note that the
17 total number of DCK pulses assigned to these additive timing values is equal
18 to $(M - N) \times G$, where $M - N$ is the number of lines which can be generated
19 within the vertical blanking interval and G is the number of DCK pulses
20 during each line interval.

21 Each additive variable is read from the memory 42 in response to a
22 corresponding line-count number and supplied to an adder 43 where the
23 additive variable is summed with an integer X , where X is the nominal value
24 of the write-in period. The binary output of the adder 43 is connected to a
25 variable rate pulse generator 44. This variable rate pulse generator may be
26 implemented with a presettable counter which increments a count number in
27 response to the DCK pulse and produces an output when that count number
28 equals some preset value, which is set equal to the output of adder 43.
29 Variable rate pulse generator 44 produces SP, VCK and DLP pulses, each of
30 which occurs at intervals varying increasingly as the row lines 11-1 ~ 11-N

1 are selected in sequence in that order. All of these variable-rate pulses have a
2 fixed time difference from one another. Initially, the variable rate pulse
3 generator 44 is activated to produce a first VCK pulse when the sync
4 generator 40 detects a frame sync.

5 The variable-rate SP and VCK pulses are supplied to the row driver 3
6 and the variable-rate SP and DLP (data latch) pulses are supplied to the
7 column driver 2 along with constant-rate DCK (dot clock) pulse which is
8 supplied from the sync detector 40. The SP and DCK pulse are also supplied
9 from the timing controller 4 to the buffer memory 5 so that stored video data
10 can be read line-by-line into the column driver 2 when a row line is selected.

11 The operation of the first embodiment of the present invention is best
12 understood with the following description with reference to the timing
13 diagram of Fig. 4.

14 As shown in Fig. 4, a frame interval is divided into a vertical scan
15 interval and a vertical blanking interval. During the vertical scan interval,
16 each of the #1 to #N line signal of a video frame is sequentially read into the
17 buffer memory 5.

18 In response to a variable-rate start pulse SP, a line signal is read out of
19 the buffer memory 5 and clocked into the column-driver shift register 20 and
20 stored in the latch circuit 21 in response to a variable-rate DLP pulse. Row
21 driver 3 selects one of the row lines 11-i in response to the same start pulse
22 and generates a gate control pulse in response to a variable-rate VCK pulse to
23 drive the selected row line 11-i. In this way, the row lines 11-1 through 11-N
24 are successively rendered active for periods T_1, \dots, T_N .

25 In the prior art, the write-in period is fixed at the nominal interval (X)
26 for all row lines. As shown in Fig. 5, the write-in periods of row lines 11-1,
27 11-2, ..., 11-N are respectively set equal to $X, X + \alpha_1, \dots, X + \alpha_{N-1}$. As a
28 result, the distance-associated different voltage drops along the column lines
29 10 is compensated. For a given write-in voltage, the light intensities of all
30 liquid crystal cells 10 are rendered substantially equal to each other.

1 Since the pulse interval can be easily controlled by the use of the
2 digital circuitry, the variable intervals of the SP, DLP and VCK pulses can be
3 precisely controlled to eliminate the undesired differences in shades of gray
4 between the top and bottom lines on the monitor screen. The precision
5 timing control is particularly important since the time assigned for each
6 write-in operation is becoming increasingly limited with the current tendency
7 toward developing high resolution, large-screen displays.

8 A second embodiment of the present invention is shown in Fig. 6. In
9 this embodiment, the write-in operations of the row lines 11-1 to 11-N are
10 respectively performed within periods $T_1 = X - \beta_1$, $T_2 = X - \beta_2$, ..., $T_{N-1} = X -$
11 β_{N-1} , and $T_N = X$, where $\beta_1 \geq \beta_2 \geq \dots$, $\beta_{N-2} \geq \beta_{N-1}$, and β_i ($i = 1, \dots, N - 1$) is
12 a subtractive timing value which varies decreasingly as a function of
13 geometric distance along the column lines between the row line 11-i and the
14 column driver 2. Therefore, the write-in period $T_i = X - \beta_i$ varies
15 increasingly, within the nominal write-in period X , as a function of the
16 geometric distance along the column lines between the row line 11-i and the
17 column driver 2. The write-in operation is thus performed within an interval
18 smaller than the horizontal line interval of the input video frame.

19 Since the write-in operation of the liquid crystal elements 13 does not
20 take longer than the time for writing the input line data into the shift register
21 20, the buffer memory of the previous embodiment is not necessary in this
22 embodiment.

23 In the second embodiment, VCK and DLP pulses are generated at
24 constant intervals and a video output enable (VOE) pulse is generated at
25 intervals increasingly variable as a function of the geometric distance from
26 the row lines to the column driver 2. In the row driver 3, each gate control
27 pulse is generated so that its begins in response to the constant-rate VCK
28 pulse and ends in response to the VOE pulse.

29 As shown in detail in Fig. 7, the timing controller 4 of the second
30 embodiment comprises a sync detector 50 for discriminating the input clock

1 and sync timing signals to detect the frame sync and line sync timing of the
2 input video frame and the dot clock pulse DCK. A constant-rate pulse
3 generator 51 responds to the detected frame and line sync timing for
4 producing a start pulse (SP), a DLP pulse and a VCK pulse at constant
5 intervals. A line counter 52, which is reset by a frame sync, increments a
6 count number each time a line sync is detected and provides a binary line-
7 count number to a memory 53. Write-in subtractive timing values β_1 through
8 β_{N-1} and "0" are stored in the memory 53 respectively corresponding to row
9 lines 11-1,, 11-N-1, and 11-N.

10 Each subtractive timing value is read from the memory 53 in response
11 to a corresponding line-count number and supplied to a subtractor 54 where
12 the subtractive timing value is subtracted from the nominal value X. The
13 binary output of the subtractor 54 is then used to preset a variable rate pulse
14 generator 55. Variable rate pulse generator 55 responds to a constant-rate
15 VCK pulse by starting the count of DCK pulses and generates a VOE pulse
16 when the count number equals the preset value.

17 The variable-rate VOE pulse and the constant rate SP and VCK pulses
18 are supplied to the row driver 3 and the constant-rate SP and DLP pulses are
19 supplied to the column driver 2 along with the input video frame (data) and
20 DCK pulse.

21 The operation of the second embodiment of the present invention
22 proceeds according to the timing diagram of Fig. 8.

23 When a line signal of the input video frame is clocked into the column
24 driver 2 in response to a constant-rate start pulse SP and latched in response
25 to a DLP pulse, the row driver 3 selects a row line 11-i and generates a gate
26 control pulse in response to a VCK pulse to drive the selected row line. This
27 gate control pulse terminates in response to a subsequent VOE pulse so that
28 the write-in period T_i for the row line 11-i is equal to $X - \beta_i$, which begins at
29 the trailing edge of the DLP pulse and ends at the leading edge of the VOE
30 pulse. In this manner, the row lines 11-1 through 11-N are successively

1 selected and rendered active for write-in periods T_1, \dots, T_N , respectively.
2 The distance-related different voltage drops along the column lines are
3 compensated and all liquid crystal cells are charged with substantially equal
4 voltages regardless of their relative positions to the column driver 2, as
5 graphically shown in Fig. 9.

6 A third embodiment of the present invention is shown in Fig. 10. This
7 embodiment is a combined form of the previous embodiments. Accordingly,
8 the timing controller 4 of the third embodiment is of similar configuration to
9 that of Fig. 3 modified according to Fig. 7.

10 As illustrated in Fig. 11, the timing controller of the third embodiment
11 comprises sync detector 60 for discriminating the input clock and sync timing
12 signals to detect the frame sync and line sync timing of the input video frame
13 and the dot clock pulse DCK. Constant-rate pulse generator 61 responds to
14 the detected frame and line sync timing for producing SP1, DLP1 and VCK1
15 pulses at constant intervals. Line counter 62, which is reset by a frame sync,
16 increments a count number each time a line sync is detected and provides a
17 binary line-count number to a memory 63. Write-in subtractive timing values
18 $\beta_1, \beta_2, \dots, \beta_{M-1}$ and write-in additive timing values $0, \alpha_{M+1}, \alpha_{M+2}, \dots, \alpha_{N-1}$
19 are stored in the memory 63 respectively corresponding to row lines 11-1, 11-
20 2, ..., 11-M-1, 11-M, 11-M+1, 11-M+2, ..., 11-N.

21 During a first portion of each video frame, each subtractive timing
22 value is read from the memory 63 in response to a corresponding line-count
23 number and supplied to a subtractor 64 where the subtractive timing value is
24 subtracted from the nominal value X. The binary output of the subtractor 64
25 is used to preset a variable rate pulse generator 66. Variable rate pulse
26 generator 66 responds to a constant-rate VCK1 pulse by starting the count of
27 DCK pulses and generates a variable-rate VOE pulse when the count number
28 equals the preset value. The variable-rate VOE pulse and the constant rate
29 SP1 and VCK1 pulses are supplied to the row driver 3 and the constant-rate
30 SP1 and DLP1 pulses are supplied to the column driver 2 along with the

1 input video frame (data) and DCK pulse. Buffer memory 5 is supplied with
2 the DCK pulse and the constant-rate start pulse SP1.

3 During a second portion of the video frame, each additive timing
4 value is read from the memory 63 in response to a corresponding line-count
5 number and supplied to an adder 65 where the additive timing value is
6 summed with the nominal value X. The binary output of the adder 65 is used
7 to preset the variable rate pulse generator 66. When the preset value is
8 reached, the variable rate pulse generator 66 produces pulses SP2, DLP2 and
9 VCK2 at variable intervals, instead of the VOE pulse. The variable-rate SP2,
10 and VCK2 pulses are supplied to the row driver 3 and the SP2 and DLP2
11 pulses are supplied to the column driver 2 along with the input video frame
12 and DCK pulse. Buffer memory 5 is supplied with the DCK pulse and the
13 variable-rate start pulse SP2.

14 The operation of the third embodiment of the present invention
15 proceeds according to the timing diagram of Fig. 12.

16 During the first portion of a frame interval, each line signal of the
17 input video frame is clocked into the column driver 2 in response to a
18 constant-rate start pulse SP1 and latched in response to a DLP1 pulse, and the
19 row driver 3 selects a row line 11-i and generates a gate control pulse in
20 response to a constant-rate VCK1 pulse to drive the selected row line. This
21 gate control terminates in response to a subsequent VOE pulse so that the
22 write-in period T_i is equal to $X - \beta_i$. In this manner, the row lines 11-1
23 through 11-M-1 are successively selected and rendered active for write-in
24 periods T_1, \dots, T_{M-1} , respectively.

25 During the second portion of the frame interval, each line signal of the
26 input video frame is clocked into the column driver 2 in response to a
27 variable -rate start pulse SP2 and latched in response to a variable-rate DLP2
28 pulse, the row driver 3 selects a row line 11-i and generates a gate control
29 pulse in response to a variable-rate VCK2 pulse to drive the selected row line.
30 This gate control pulse terminates in response to a subsequent VCK2 pulse so

1 that the write-in period T_i is equal to $X - \alpha_i$. In this manner, the row lines 11-
2 M through 11-N are successively selected and rendered active for write-in
3 periods T_M, \dots, T_N , respectively.

4 As shown in Fig. 13, the write-in periods for row lines 11-1 to 11-M-1
5 are $T_1 = X - \beta_1, T_2 = X - \beta_2, \dots, T_{M-1} = X - \beta_{M-1}$, respectively, and the write-
6 in periods for row lines 11-M to 11-N are $T_M = X, T_{M+1} = X + \alpha_1, \dots, T_N = X$
7 $+ \alpha_{N-1}$, respectively, where $\beta_1 \geq \beta_2 \geq \dots \geq \beta_{M-1}$ and $\alpha_1 \leq \alpha_2 \leq \dots, \alpha_{N-2} \leq$
8 α_{N-1} .